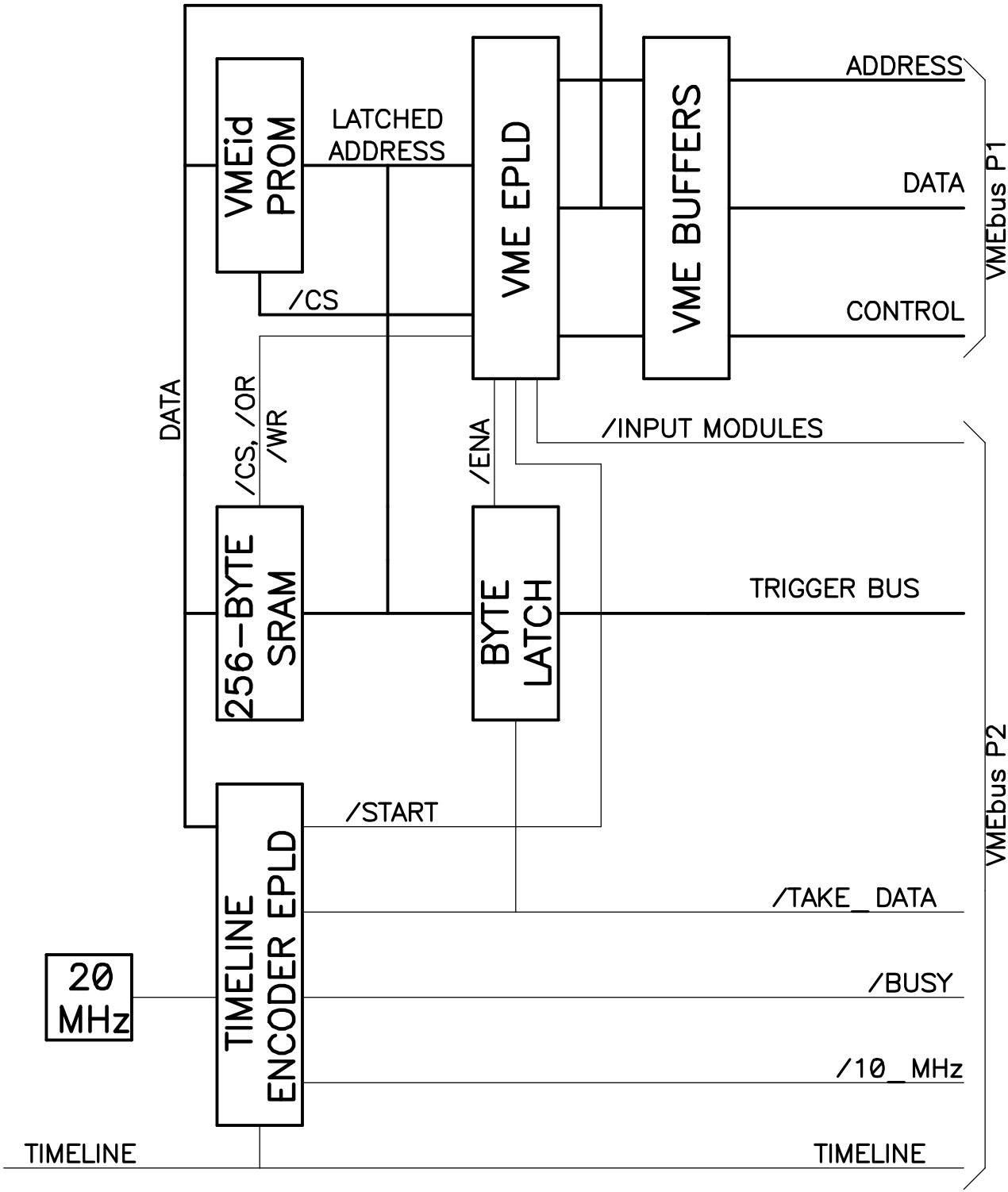
VMEid PROM
LATCHED ADDRESS
VME EPLD
VME BUFFERS
ADDRESS
DATA
CONTROL
VMEbus P1
/CS
DATA
/CS, /OR
/WR
/ENA
/INPUT MODULES
256-BYTE SRAM
BYTE LATCH
TRIGGER BUS
VMEbus P2
/START
TIMELINE ENCODER EPLD
/TAKE_DATA
20 MHz
/BUSY
/10_MHz
TIMELINE
TIMELINE