12-Sep-01
Test Procedure for the Rhic Real Time Data Link Encoder Board
Schematic #94028013

Equipment Used:
- Fluke hand held Digital Multimeter
- 2 Channel Oscilloscope
- 2 Oscilloscope Probes
- Logic Analyzer
- Real time Timing System
- Pulse Generator (up to 10KHz)
- 2 BNC terminated coax cables
- Dumb Terminal
- 6U VME Extender Board
- MVME162 Processor Board with VXWorks proms installed
- Rhic Real Time Data Link Dual Channel Input Board 94028014
- Specification for the RHIC RTDL system 10/27/93 REV. 4.1
- RTDL Monitor

I. General Inspection and Set-up

1.) Before applying power to the board:
   a. check all IC's for proper insertion (no bent under pins), proper device type and orientation.
   b. check for proper polarity on electrolytic capacitors.
   c. check for shorts from +5 to ground with ohm meter.
   d. check all values on analog parts, resistors, capacitors, etc.
   e. check resistor sips for proper orientation and value.
   f. check for solder bridges on connectors and pin grid arrays.
   g. check for proper orientation of sip delay line.

2.) Program all programmable devices: (hartmann\altera\rtdl)
   a. U3- EPM5032-25 Filename 94028021.gdf (hartmann\altera\timing\rclkdec2.gdf)
   b. U6- PLS153N Filename 94028023.jed (hartmann\pld\rhic\tmevntdc.jed)
   c. U7- EPM7128GC-20 Filename 94028020.gdf (\encode40\rhicrtdl.gdf)
   d. U20- 82S123 Filename 94028017.hex (hartmann\pld\rhic\statid0.hex)
   e. U21- 82S123 Filename 94028022.hex (hartmann\pld\rhic\statid1.hex)
   f. U26- EPM7128GC-20Filename 94028019.gdf (\encode40\vmeinreg.gdf)

   94028022 (Statid1.hex) must be modified individually for each board to include the major revision level, the minor revision level and the board serial number.

3.) Power board on. Check +5 to ground at different points around the board. Make sure all points are >= 4.75 and <= 5.25. Power board off.

4.) Insert all programmable IC's into the proper sockets, checking for proper orientation and proper insertion.

5.) Jumper the board for VME base address of 200h:

E16 - E24	msb	IN
E15 - E23		IN
E14 - E22		IN
E13 - E21		IN
E12 - E20		IN
E11 - E19		IN
E10 - E18	lsb	OUT

6. SW1

Switch 1	OPEN
Switch 2	CLOSED
Switch 3	CLOSED
Switch 4	CLOSED

```
Switch 5    CLOSED
Switch 6    CLOSED
Switch 7    CLOSED
Switch 8    OPEN
```

II. VME Test

1.) Connect the terminal to the front panel db25 connector on the MVME162 processor board.

2.) Power on chassis and terminal.

3.) Processor should prompt with '->'.
This board occupies 512 bytes of memory space. The lower 256 bytes contain the status/id bytes (64) (read only), the command register (read/write), the status register (read only), and the interrupt vector register (read/write). The upper 256 bytes contain the Parameter ID codes. There are 255 valid ID codes (00 is illegal).
To read the first 256 bytes of memory, at the prompt type:
d 0xffff0200,256,1
The first 64 bytes are the VME ID and board related information. This data is configured as '2E' (ASCII period) in all even locations, and data (ASCII text) in all odd locations. Display should show:

```
ffff0200      2E56 2E4D 2E45 2E49 2E44 2E42 2E4E 2E4C   .V.M.E.I.D.B.N.L
ffff0210      2E56 2E31 2E30 2E35 2Exx 2Exx 2Exx 2Exx   .V.1.0.5.x.x.x.x
ffff0220      2Exx 2Exx 2Exx 2Exx 2Exx 2Exx 2Exx 2Exx   .x.x.x.x.x.x.x.x
ffff0230      2Exx 2Exx 2Exx 2Exx 2Exx 2Exx 2Exx 2Exx   .x.x.x.x.x.x.x.x
ffff0240      FF00 xxxx FFxx FFFF FFFF FFFF FFFF FFFF   ................
ffff0250      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffff0260      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffff0270      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffff0280      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffff0290      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffff02A0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffff02B0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffff02C0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffff02D0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffff02E0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
ffff02F0      FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF   ................
```

4.) Command Register: ffff0240.
Read: d 0xffff0240,10,1
Write: m 0xffff0240
Each of the low order 8 bits should be toggled on and off one at a time to verify writing to and reading from that register.
To set bit 0, at the prompt type: m 0xffff0240↵
Response: ffff0240 -
Type: 0001↵ (This should set bit 0.)
To end write: .↵
To read: d 0xffff0240↵
Verify that bit 0 was set.
To clear bit 0, at the prompt type: m 0xffff0240↵
Response: ffff0240 -
Type: 0000↵ (This should clear bit 0.)
To end write: .↵
To read: d 0xffff0240↵

All other low order bits (0-7) should be set in this way. Once all of the command bits have been checked, write a '0000' to the command register. Verify its contents.

5.) Status Register: ffff0242. (16 bit register)
The upper 8 bits are undefined. Read the contents and verify the current status of the board. (Normal status = 1C) Refer to the RHIC RTDL System Specification for bit definitions.

6.) Interrupt Vector Register: ffff0245 (8-bit register)
Set the contents of this register to 40H. Verify that this location contains 40H.

7.) Interrupts

a. To initialize registers and FEC:

```
cd"/home/cfsa/hartmann/vx"↵
ld <intst1.o↵
intConnect(4*0x40,intst1)↵
```

b. To set the interrupt level:

```
sysIntEnable(n)↵   (n=1-7)
sysBusIntGen(n,0x40)↵
m 0xffff0240 00y8↵      n=1,y=2
                        n=2,y=4
                        n=3,y=6
                        n=4,y=8
                        n=5,y=A
                        n=6,y=C
                        n=7,y=E
```

Set the interrupt vector register to 40H.
To generate a level 1 interrupt, n=1 and y=2. Check all interrupt levels: 1-7.
For each interrupt verified, code in (b) above must be re-entered.

To generate an interrupt, disconnect the Event Link Input.

8.) Parameter RAM: ffff0300. (256 bytes)
Must be initialized with a list of parameter ID codes. The Parameter ID Code List must be loaded into memory one byte at a time and the list must terminate with a '00' as the last entry.

```
Read: d 0xffff0300,256,1
```

This returns 256 bytes of memory one byte at a time.

```
Write: m 0xffff0300,1↵
       01↵
       02↵
       03↵
       04↵
       05↵
       06↵
       .↵
```

This loads the parameter ID codes 01, 02, 03, 04, 05, and 06 into the SRAM.

III. General Functionality Test

1.) Connect Real Time Timing System cable to front panel twinax connector labeled "EVENTLNK". Power board on.

2.) Terminate the EXTTRIG input with a 75 ohm termination.

3.) Front panel indicator "EVENTLNK" should be lit. If U6 is programmed properly, front panel indicator "EVENT" should also be lit. If this is not the case, make sure that both the RESET and EXTERNAL TRIG ON/OFF commands are both '0'.

```
Type: d 0xffff0240↵
```

Verify that both the RESET and External Trigger Enable Commands are set to '0'by referencing system specification. If not, set them both to '0'.

```
Type: m 0xffff0240↵
      0000↵
```

Set the GO bit in the command register.

```
Type: m 0xffff0240↵
      0004↵
      .↵
```

The "LDDATA" front panel indicator should now flash at the same rate as the "EVENT" indicator.

4.) Monitor the link output by connecting one channel of the oscilloscope to the LEMO connector labeled "BUFRTDL" through one of the coax cables with a 75 ohm termination. The scope should display a 10MHz square wave. In addition, the front panel indicator labeled "RTDL" should be lit.

5.) a. Connect the logic analyzer to the IDCODE[7..0] bus (U24). Connect the trigger clock for the pod to the ASACK0/ signal: U10-12. Verify that there are the same number of codes as are programmed into the SRAM.
b. Set the External Trigger Enable bit to '1'.

```
Type: m 0xffff0240↵
      0006↵
      .↵
```

Connect a trigger pulse not to exceed 10KHz to the EXTTRIG input. Verify that the EXTTRIG led is lit. Connect the trigger clock for the pod to U33-6. Verify that there are the same number of codes as are programmed into the SRAM. Reset the External Trigger Enable bit to '0'.

```
Type: m 0xffff0240↵
      0004↵
      .↵
```

6.) Connect one scope probe to the EVNT720 signal, U6-19, and the other probe to U8-20, the output enable of the Parameter ID RAM. Trigger the scope on the EVNT720 signal. There should be one active lo pulse for each code every 1.5us for each trigger event.

7.) Connect one scope probe to U8-20, and connect the other probe to U24-11, NOREPLY. Trigger the scope on U8-20. Verify that NOREPLY is latched on the occurrence of the first parameter that does not respond. Status Register should show contents of 011CH.

```
Type: d 0xffff0242,10,1↵
```

Verify contents by referencing system specification.

IV. General System Test

1.) Power chassis down. Set the base address of a tested Rhic Real Time Data Link Input Board, Schematic #94028038, to F7h as follows:

```
Jumper  E32 to E40.
```

Set Parameter ID for Channel 1 to 7Fh as follows:

```
Jumper E71 to E79.
```

Set Parameter ID for Channel 2 to FCh as follows:

Jumper E99 to E107
E100 to E108.

Plug Input Module into the VME backplane.
Plug RTDL Monitor into the VME backplane. Connect a twinax cable from the RTDL output of the V105 Module and the RTDL Input of the RTDL Monitor.
Power up chassis.

2.) Via the monitor, download a parameter value to both channels.

```
Type: m 0xffff7f40↵
      0006↵       (Halt/VME Mode Ch1)
      0006↵       (Halt/VME Mode Ch2)
      0102↵       (Ch1 VME Data)
      xx03↵
      abcd↵       (Ch2 VME Data)
      xxef↵
      . ↵
      m 0xffff7f40↵
      000a↵       (Go/Load Ch1)
      000a↵       (Go/Load Ch2)
      . ↵
```

Refer to the System Specification for further details on configuring this board.

To Re-initialize the V105 (Encoder) Module:

```
Type: m 0xffff0240↵
      0004        (G0)
      . ↵
```

3.) Data Verification.

To verify that the data on the link is the same as the downloaded data, dial in the Parameter ID Code, 7F, on the thumbwheel switch labelled “Code Select”, and set the toggle switch in the “Code” position. Set the “Stop On” switch to “No Stop”. Press the “Reset” button. The data that was loaded above for this Parameter ID Code should be displayed (030102). Repeat for Parameter ID Code FC.