

# THE DATACON MASTER - RENOVATION OF A DATACON FIELD BUS COMMUNICATIONS SYSTEM FOR ACCELERATOR CONTROL\*

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## *Abstract*

The Datacon Master (V110) is a custom-designed VMEbus SBC event driven serial communications engine featuring a superscaler RISC 32-bit Intel i960 CPU. The V110 and a commercial VMEbus host CPU running vxWorks with an Ethernet LAN connecting UNIX workstation consoles, make up the real time control system. Five V110 and three host CPUs will replace and upgrade PDP10 and PDP8 Datacon AGS front end computers. Five V110s will support twenty Datacon field busses with some 2600 devices. The V110 firmware is written in C. An accelerator event time link interface and  $\mu$ S timestamp are built-in. Each Datacon field bus supports up to 256 devices on a multidrop RG62A/U coaxial cable with up to 2000 feet between repeaters. Each V110 drives up to four full Datacon field busses at 1 MHz bandwidth.

## I. INTRODUCTION

The Datacon system is a serial coaxial transformer isolated communication field bus system used to control and monitor accelerator remote devices. The Datacon field bus has been a BNL accelerator standard since its initial use in 1965.

### A. *Why Renovate?*

The forcing factor to renovate was the inability to repair the aging PDP-8E and PDP10 computers. The maintenance on this aging system was costly and the large number of accelerator devices dependent on the Datacon system could not be converted in a reasonable period of time to a new modern field bus.

### B. *Upgrading to a Real Time Object Oriented Solution*

The changeover to a new system had to be done quickly and cleanly. With as many as 2600 existing accelerator devices to control and monitor, a compatible and well-defined solution was required which could literally plug into the existing Datacon field bus coaxial cables. The limited time available during maintenance cycles was all that was available to change over to and qualify a new system. A well vetted and low risk system architecture [1] and strategy had to be developed. As a control system was being designed for the Relativistic Heavy Ion Collider (RHIC), the decision to merge this real-time object-oriented architecture with the Datacon field bus was reached.

### C. *The Solution*

A commercial VMEbus host CPU mated with a custom designed VMEbus SBC event driven serial communications engine featuring a superscaler RISC 32-bit Intel i960 CPU met the design challenge. The commercial VMEbus host runs the vxWorks [2] real-time operating system and connects to UNIX workstations over a Ethernet [3] LAN. The V110

Datacon Master is the custom designed front end computer that integrates an accelerator event link system [4] with accelerator devices for up to 8 users adding new capabilities. The V110, with multiple user capability, increased bandwidth, shorter latency and overhead, would outpace the original system in functionality and performance by at least an order of magnitude. Great improvements came from a robust set of supported network protocols allowing even engineering PCs to be used to develop and test complex control system components. As communications improved and performance issues were no longer the limiting factor driving accelerator devices, a jump in controls effectiveness and efficiency could be realized.

## II. SYSTEM COMPONENT DESCRIPTION

The Datacon Master System is divided into five functional parts.

### A. *The Commercial VMEbus Front End Computer*

A Motorola MVME 162-222 was selected for use in the Datacon Master System for compatibility with the large quantities of this SBC previously selected for the new RHIC control system. The MVME162-222 with the vxWorks real-time operating system provided an adequate platform for the FEC functionality required to support Datacon Master functionality as well as being well positioned to make best use of resident programming skills.

### B. *The V110 Datacon Master Serial Communications Engine*

The V110 is a single board VMEbus compatible custom designed communications engine. The V110 includes an accelerator event link decoder, a  $\mu$ S time stamp counter, 4 parallel ports for 4 individual Datacon field busses, a full featured VMEbus interface which includes block transfer capability, 2 Mbytes of fast static RAM, a 33 MHz 32-bit Intel i960 RISC superscaler  $\mu$ P, five large custom designed Altera programmable logic devices and 32-bit fast burst access PROM.

### C. *The P110 P2 Buffer Board*

The P2 Buffer Board connects the VMEbus back plane to a ribbon cable assembly via buffers to allow high speed signals to travel over ribbon cable assemblies to the T110 Datacon Master Transition Module.

### D. *The T110 Datacon Master Transition Module*

The T110 Datacon Master Transition Module contains 4 large Altera programmable logic devices that provide the serialization from a 32-bit wide multiplexed high speed data bus to the relatively slow 1 MHz serial data stream. The Altera devices send and receive TTL level serial differential data to the Datacon Driver.

\*Work Performed under the auspices of the U.S. Department of Energy.

### E. The DD110 Datacon Driver

The DD110 Datacon Driver converts the differential serial TTL level data found on the T110 DCM Transition Module into the  $\pm 15$  Volt levels transmitted and received on the Datacon field bus coaxial cables. The DD110 is located in its own rack mountable enclosure with its own power supply to isolate Datacon electrical noise from the rest of the Datacon Master system.

## III. SYSTEM OPERATIONAL REQUIREMENTS

The renovated system must be compatible with all accelerator devices that predated it. There are approximately 28 device types. A recent survey found 2616 active addresses. Some of the 28 device types are power supply controls, stepping motor positioning systems, collimator jaw positioners, beam profile monitors, scalers, autodets, analog signal acquisition, video multiplexing, function generators, and chipmunk radiation monitors. A comprehensive plan to port over drivers and integrate the new real-time operating system was devised. Creation of a test platform with real Datacon devices and loop back testing would answer most of the compatibility issues facing the cut-over to the new system. Persistence of software objects would have to be added to the new system for power dips or outages. Integration with the new accelerator event link would require some development and coordination in both hardware and software. The firmware for the V110 Datacon Master would have to be developed jointly between the hardware designers and the software group. A specification for the host front end computer to the V110 Datacon Master had to be developed which was flexible and broad enough to accommodate both single user machines such as RHIC and multiple user machines such as the LINAC, the BOOSTER, and the AGS. The Datacon Master was designed to allow modular additions to the existing Datacon field bus controls. Up to 8 V110 Datacon masters accommodating 32 Datacon field lines could be accommodated in a single VME chassis. Power savings over the original main frame PDP10 and PDP8 computers with two 20-ton and one 5-ton air conditioning units would not be insignificant.

### A. Integration Testing

A series of stress tests were created to run the new Datacon Master system at full bandwidth in conjunction with a test set that looped back transmissions for testing the error rate and qualifying both hardware and software. Tests were devised which were event link controlled as well as load and go immediately. The insertion and extraction of devices from chains of linked lists was tested using the host and Datacon Master firmware. Thousands of operations could be tested with the loop back features while looking for data failures or scheduling failures or overlaps. The event link code table acts as an event code filter and is maintained by the Datacon Master  $\mu$ P. Codes designated as active are downloaded from the host front end computer. Any and all codes may be used as an event code, fiducial, or user change. The interpretation of the codes is completely under tabular program control. Connection to the real event link line demonstrated the proper dispatching of chained commands. Active event link codes are stored in a FIFO such that any code arrival rate can be handled properly. A Workstation was used to dispatch and display the reply messages with  $\mu$ S arrival time stamps and

any DNA (Did Not Answer) status for unconnected devices after a preset  $\mu$ S time-out period. Time-out periods were preset and observed on a line by line basis. On board non-volatile RAM may be used to safeguard against power interruption. The Datacon Master re-initializes within 1 second of power restoration.

### B. Throughput or Performance

No significant degradation in system performance will be permitted with 4 lines simultaneously operating at the highest permissible bandwidth supported by the Datacon Line Specification [5]. All overhead for processing and time sharing with the VMEbus must be included in the serial shift out time of the Datacon transmission. Latency time from an event occurrence to the beginning of a Datacon transmission shall not exceed 25  $\mu$ S with 4 lines operating at maximum bandwidth. The Datacon Master was designed to modularly replace the Transition Module with a fiber optic driver such that upgrading to fiber can be accomplished with minimal impact on system design.

The time-out may be individually tuned to each line to provide the fastest possible turnaround time in the presence of a missing device. The time-out period is a function of line length, number of repeaters used, and device requirements.

The main memory consists of 2 Mbytes of high speed static RAM. This is enough RAM to support several users with long chained sequences of command and response messages. The memory is dual ported between the  $\mu$ P and the VMEbus. Bus arbitration logic grants the  $\mu$ P access to the SRAM on a priority basis before the VMEbus, which still allows enough time to complete all VMEbus cycles during idle  $\mu$ P bus times. VMEbus block transfer capability to SRAM provides adequate VMEbus bandwidth when multiple Datacon Masters are inserted in a VME chassis. Eight general purpose registers are dual ported to the  $\mu$ P and to the VMEbus for passing semaphores and status. Global and module switch registers are used to interrupt the local processor from the VMEbus.

## IV. SYSTEM ARCHITECTURE

### A. EPROM

The 64 Kbytes of EPROM are arranged 32-bits wide by 16 K deep. The EPROM is a burst access variety that makes use of the pipelined burst access mode of the i960. This is a high throughput memory region programmed with zero wait states for 132 Mbyte per second transfer rates, the highest performance available in a commercial  $\mu$ P at the time of the Datacon Master design.

### B. Superscaler RISC Processor

The Intel A80960CA-33 is a 33 MHz  $\mu$ P with superscaler technology that enables the  $\mu$ P to execute up to three instructions per clock cycle. The  $\mu$ P has a two-way set associative 1 Kbyte 32-bit wide zero wait state internal instruction cache, a 32-bit wide 1 Kbyte zero wait state internal data RAM, 5-15 set register cache, and a high speed vector cached interrupt controller. The bus control unit allows the main external static RAM region to be configured as big endian for compatibility with dual porting to the VMEbus, while keeping  $\mu$ P specific externals such as EPROM and its firmware little endian for compatibility with Intel compilers and software development tools.

### C. 2 Mbytes SRAM

The 2 Mbytes of SRAM is configured as 32-bit wide by 500 K deep. It is in a pipelined burst memory region with one wait state. The SRAM is dual ported with bus arbitration to the VMEbus and is configured as big endian for compatibility with 68000 addressing.

### D. Accelerator Event Link Decoder Filter

The event link decoder filter is set up as 8 pages in static RAM to accommodate 8 possible users. The memory table may be updated by the local  $\mu$ P and then page swapped on the arrival of a event link fiducial code that signifies a user change.

### E. Priority Interrupt Control Logic

To efficiently prioritize incoming Datacon line data available, parity error and time-outs for the 4 Datacon lines serviced plus VMEbus requests and VMEbus register interrupts, VMEbus error, and event link interrupts, custom interrupt control logic was designed to allow maximum throughput with minimum latency.

### F. Event Link FIFO

Accelerator events may arrive back to back or 1.2  $\mu$ S apart. To handle this possibility, an event link FIFO temporarily stores each event until the  $\mu$ P can service the interrupts that nominally take a few  $\mu$ S.

### G. NVRAM

NVRAM is available for storing volatile data to handle power dips. The Datacon Master finishes initialization after a power dip in about 1 second. This avoids the long host computer boot up time lag.

### H. I/O Functions, Watchdog, Time Stamp

A watchdog monitors the voltage on the Datacon Master power planes. If the voltage should dip to 4.5 volts the watchdog reinitializes the local  $\mu$ P, which then reinitializes the on board logic and VMEbus interface. This ensures an orderly power on reset as well as power dip reset. An early AC fail condition interrupts the  $\mu$ P at the highest priority and saves volatile data. The watchdog is pinged by the local  $\mu$ P as part of normal firmware operation. Should the  $\mu$ P halt or hang, the watchdog would reset the  $\mu$ P and reinitialize the board.

### I. Timer Counters

Four timer counters are used to control the time-outs for each Datacon line. The 1  $\mu$ S clock on the timer counters provides delays up to 512  $\mu$ S programmed in 2  $\mu$ S increments. These counters ensure minimal turnaround time should a field device be disconnected or fail.

## V. FIRMWARE

The Datacon Master protocol defines four types of information blocks: Input Request Blocks, Message Descriptor Blocks, Source Message Blocks, and Reply Message Blocks. IRBs are created by an off board host and are used to append or delete SMBs via a linked list of pointers in the MDB. IRBs contain a PPM user, accelerator event code,

Datacon line number, and MDB pointer. The MDB chains together SMB and RMBs that are executed on the same accelerator event. MDBs contain a forward and backward linking pointer, a SMB element count, a RMB repeat index, a SMB pointer and RMB pointer(s). SMBs and RMBs are therefore dynamically linked which gives rise to an efficient method for making modifications with little overhead. This technique allows multiple buffering, and complex triggering sequences to be created. MDB may be efficiently cut and pasted using the linked list of pointers. RMBs contain a start time stamp, end time stamp, reply message, and status code. The off board host is responsible for memory management and is required to secure exclusive use of sufficient memory space for each of the SMBs and RMBs that the host creates. For space reasons this protocol description has been oversimplified.

## VI. ACKNOWLEDGMENTS

The authors are indebted to J. Skelly for driver software development and his ideas and contributions toward the design specification, and to T. Clifford and B. Oerter for their helpful discussions on system implementation. Special thanks to N. Schumberg for his contributions to the DD110 and T110 designs and R. Warkentien for firmware development.

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