

VECTOR FUNCTION GENERATORS

AGS

AC TECHNICAL NOTE

NO.

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1. Introduction

When thinking of how to best control the main ring power supplies(MRPS) for the Booster dipole magnets it was decided that a promising approach was through vectorization of analog functions. This is because vectors are not difficult to generate, they reduce the amount of information that is necessary, and hence reduce network transmission time and the storage requirements. The latter enabled locating the hardware in remote racks close to the power supplies. The disadvantage of this is that specialized hardware is required to convert each vector to a string of setpoints.

2. Vector Definition

Each vector is represented by 4 16-bit words. There is an initial value (I), a slope (M), a duration (N), and a control word (C).

The initial value defines the first setpoint for each vector. Even though it is redundant it does cause self correction if there is a vector implementation error. It is also useful for applications where waveform discontinuities are required.

The slope (M) is a 12-bit value with an extra sign bit. Two bits are set aside to improve the slew rate by a factor of 16 or 4. This is done at the expense of DAC resolution by downsizing the 16-bit counter to 12 and 14 bits respectively. The last bit(enable/inhibit) is used for device specific applications. The slope is defined as $M/4096(\text{CLK})$ where M is an integer and CLK is a 1MHZ clock that is synchronized to T0.

The duration (N) is a 16-bit value which defines the length of each vector. With a 1MHZ clock it can vary from 1 usec to 65 msec.

The control word (C) has 2 write and 16 read bits. The write bits run/stop and vector interrupt identify the last vector(stop) and all others(run) and when to make a vector respond to an external time or gauss event. If the event precedes the completion of the vector the hardware advances to the next vector and if the vector completion precedes the event the hardware stops until the event occurs. Fourteen of the read bits define these two conditions. One defines which condition, 12-bits define the delta T between the event and vector completion time(4 msec max.) and the last bit identifies when delta T is greater than 4msecs.

There is a maximum of 256 vectors and the number of vectors is a variable which is defined by the first vector with a stop bit. Thus a DC function requires a single vector.

3. Hardware Implementation

There are 3 hardware units. The Vector Amplitude Module which processes the initial and slope values and generates the analog output via a 12-bit DAC. The Vector Duration Module which processes duration and control values to generate a vector clock and vector advance for the amplitude module. The TTL to Fiber Optic Module transmits the 2 timing signals from the duration to the amplitude modules via fiber cables. The later has 14 channels and hence 1 duration module can control up to 7 amplitude modules through 1 fiber optic module. Multiple duration modules can share a fiber optic module to control independent power supplies.

The amplitude module has a datacon interface and the duration module has a multibus interface. The amplitude module also supports a 16-bit interface to an external 16-bit DAC.

4. Hardware System Overview

Each of the 2 modules has an identical memory structure. There are 256 times 2 words of storage to implement each function in each. Since it is possible to have common timing for multiple functions, this results in an economy in hardware and tables in duration modules.

Since all current systems support PPM, each of 4 users has a separate table. The hardware actually supports 8 active users. In addition each table is doubled buffered so that there is an active table for processing and an inactive table for loading new functions. Total memory capacity is thus 256(vectors) by 2(I and M or N and C) by 8(PPM) by 2 equals 8192 words of memory per module. All memory chips are dual ported to support simultaneous memory access to both the vector processor and the device controller.

Each module has an 8-bit mask register which identifies the active/inactive status of each table. All tables in all modules are maintained in parallel.

All timing is synchronous with the time line generator. Each active user code, in conjunction with the mask, selects its table address. At each T₀ time the first vector of the selected table is read and implemented. In parallel the duration module is supplying vector clock(1 MHZ) and vector advance to the amplitude module while it is jamming I into a 16-bit up/down counter. It generates M/4096 x vector clock, and drives the counter which is the input to the DAC. This continues until the next vector advance which increments the table address by one. This process continues until a stop vector is implemented. The duration module stops sending clocks and

advances. All connected amplitude modules stay at the last table address and counter value until a subsequent T0. If a new user code is detected the table address is changed prior to T0. The 1MHZ clock, T0, Prepulse and the User codes are all the required timing line signals.

While this is transpireing, a new function can be loaded into the inactive memory. When this is complete for all duration and amplitude modules, the control software, uses an event(Prepulse) prior to T0 to update all mask registers. Whereupon at T0 the inactive becomes active and vice versa. The new vector process then commences for the appropriate user.

For those vectors which have the vector interrupt turned on in the duration module, the vector process is conditioned by the occurrence of a time or gauss line event. It determines when the subsequent vector is processed independent of the hardware. If the event never occurs, after the start of the same vector, there is a "stopage" until the next T0.

5. Software System Overview

The software support comes from two levels, local and high level. The local level has to manage the memory tables in real time for PPM applications and the high level generates the vectorized functions.

Usually, the high level software has knowledge of the needed functions. A vectorization algorithm converts this information into a string of vectors which doesn't exceed 256 and is consistent with the aforementioned vector format. For those applications where a duration module controls multiple amplitude modules, the program has the added constraint of common timing for different functions.

The local software takes the string of vectors and stores them in tables by user. It updates the mask and in real time switches the buffered tables. It also allows the application code to read and write all tables.

6. Miscellaneous Comments

All systems in the field use the 1MHZ clock as the basic unit of time for function generation. The exception is the Siwemen's MG set which has a 500KHZ clock. This was done to lengthen the maximum vector duration to 130 msec to conserve vectors during flattops.

There are two systems in the field which generate synthetic gauss clocks. This was implemented by having an application program vectorize a real B field, transmitting this information to one function generator, and utilization of the internal vector process signals. The slope of each vector is a measure of the rate of change of the magnetic field. Therefore the signals $(M)CLK/4096$, its associated sign bit, and the appropriate data base scaling produced the synthetic gauss clock.