

1.0 TEST PROCEDURE - MODULE ASSEMBLY D09-E2587-E2588-E2613	1
1.1 The Module Drawings are:	1
1.2 Hazards	2
1.3 Initial tests V196, V197, & V198	2
1.4 Program/verify programmable integrated circuits	2
1.4.1 Testing Suspect EPLDs	3
1.5 Component installation	4
1.6 Initial power application.....	4
1.7 Initial V100 Timeline Encoder Module VMEbus tests.....	6
1.7.1 V196 AGS Timeline Decoder Module tests.....	6
1.7.2 V197/V198 AGS Timeline Trigger/Buffer Module tests.....	8

1.0 TEST PROCEDURE - MODULE ASSEMBLY D09-E2587-E2588-E2613

1.1 The Module Drawings are:

V196 AGS TIMELINE DECODER MODULE

- * D09-E2587 Module Assembly - V196 AGS Timeline Decoder Module
- D09-E2551 Front Panel Detail & Assy - V196 AGS Timeline Decoder Module
- D09-E2550-3 PWB Assembly - V196 AGS Timeline Decoder Module
- D09-E2549 PWB Drilling - V196/V197/V198 AGS Timeline Modules
- D09-E2548 Schematic - V196/V197/V198 AGS Timeline Modules
- PLD200-x AGS Event Trigger Decoder - V196/V197 AGS Timeline Modules

T196 AGS TIMELINE MODULE TRANSITION MODULE

- * D09-E2610 T196 AGS Timeline Buffer Module Assembly
- D09-E2609 T196 AGS Timeline Buffer Module Front Panel Drill & Screen
- D09-E2608 T196 AGS Timeline Buffer Module Schematic

V197 AGS TIMELINE TRIGGER MODULE

- * D09-E2588 Module Assembly - V197 AGS Timeline Trigger Module
- D09-E2552 Front Panel Detail & Assy - V197 AGS Timeline Trigger Module
- D09-E2550-2 PWB Assembly - V197 AGS Timeline Trigger Module
- D09-E2549 PWB Drilling - V196/V197/V198 AGS Timeline Modules
- D09-E2548 Schematic - V196/V197/V198 AGS Timeline Modules
- PLD200-x AGS Event Trigger Decoder - V196/V197 AGS Timeline Modules

V198 AGS TIMELINE PARALLEL BUFFER MODULE

- * D09-E2613 Module Assembly - T198 AGS Timeline Buffer Module
- D09-E2612 T198 AGS Timeline Buffer Module Front Panel Drill & Screen
- D09-E2611 T198 AGS Timeline Buffer Module Schematic
- * D09-E2589 Module Assembly - V198 AGS Timeline Parallel Buffer Module
- D09-E2553 Front Panel Detail & Assy - V198 AGS Timeline Parallel Buffer Module
- D09-E2550-1 PWB Assembly - V198 AGS Timeline Parallel Buffer Module
- D09-E2549 PWB Drilling - V196/V197/V198 AGS Timeline Modules
- D09-E2548 Schematic - V196/V197/V198 AGS Timeline Modules

V198-V197 installation requires backplane assembly
94028031 PWB Assembly - Timeline Encoder Module Backplane

T198 AGS TIMELINE MODULE TRANSITION MODULE

- * D09-E2613 T198 AGS Timeline Buffer Module Assembly
- D09-E2612 T198 AGS Timeline Buffer Module Front Panel Drill & Screen
- D09-E2611 T198 AGS Timeline Buffer Module Schematic

IEEE P1014 VMEbus Specification

1.2 Hazards

By themselves, the AGS Timeline Modules don't use or contain any hazardous voltages or materials.

1.3 Initial tests V196, V197, & V198

REQUIRED EQUIPMENT:

- 1 - 3X magnifying glass
- 1 - multimeter

Following assembly, prior to plug-in component installation, perform the following tests:

- a. Using assembly drawings:
 - V196 D09-E2550-3 & D09-E2587
 - V197 D09-E2550-2 & D09-E2588
 - V198 D09-E2550-1 & D09-E2613

Visually inspect each module for proper assembly and component placement.

- b. Using schematic drawing, D09-E2548, test for shorts between the GROUND and POWER planes.

C23-24 leads are a good place

- c. Using schematic drawing, D09-E2548, check that the following pins are not connected to GROUND or POWER.

- +5V STANDBY P1B21
- +12V P1C31
- 12V P1A31

1.4 Program/verify programmable integrated circuits

REQUIRED EQUIPMENT:

If programming MAX7000 or MAX7000E

- 1 - IBM PC with Altera programmer attached
- 1 - Altera personality module PLMJ7128-84-00

If programming MAX7000S

- 1 - IBM PC with Altera BitBlaster programmer
- 1 - Kerner VME DEBUGGING ISOLATION BOARD, Assembly D09-E2386-5
- 1 - Current limiting 5 VDC, 5A power supply
- 1 - PLCC removal tool such as QILEXT-1

NOTE: The V198 modules doesn't contain any programmable integrated circuits.

NOTE: The V196 & V197 modules will accept Altera 7000, 7000E, or 7000S parts. The Altera programmer will identify the parts 7000, or 7000E automatically. The 7000S part are programmed in-system with the serial BitBlaster.

NOTE: Both the V196 & V197 use a PLD200-x, however each modules PLD-200-x is different. The difference is the dash number: example PLD200-1 is different from PLS200-2. The difference is in the event codes detected.

- a. If using the Altera programmer, use the PC with the Altera programmer module attached. Altera MAX+PLUS II is a WINDOWS program. In WINDOWS:

1. Click on the MAX+PLUS II icon.
2. For each new EPLD, click on FILES, PROJECT, NAME. Then enter the project named below.
3. Click on MAX+plus II for function menu.
4. Click on PROGRAMMER, the programmer window will appear. After it is initialized, the window will display the PROJECT name, and the EPLD checksum.
5. Insert an EPLD in the programmer, and click on PROGRAM, or depress the START button on the programmer. Continue until all

EPLD's are programmed.

6. Go to step 2 for EPLD's with different PROJECT names.

- b. If using the BitBlaster, insert an Altera EPM7128SLC84-3 in U10.
 - 1. Test for a short between the GROUND and +5V planes using C23-24 leads.
 - 2. Set the Kerner VME DEBUGGING ISOLATION BOARD current limiting power supply to 5VDC @ 2A. The module and BitBlaster are powered by the power supply during programming.
 - 3. Insert the module in the Kerner VME DEBUGGING ISOLATION BOARD, and attach the BitBlaster connector to J18.
 - 4. Turn on power supply, the module LEDs may flash, and the BitBlaster power led will illuminate.

- c. Use the PC with the Altera BitBlaster attached. In WINDOWS:
 - 1. Click on the MAX+PLUS II icon.
 - 2. For each new EPLD, click on FILES, PROJECT, NAME. Then enter the project named below.
 - 3. Click on MAX+plus II for function menu.
 - 4. Click on PROGRAMMER, the programmer window will appear. After it is initialized, the window will display the PROJECT name, and the EPLD checksum.

NOTE: If BitBlaster is not selected, in PROGRAMMER under OPTIONS, HARDWARE select the BitBlaster.

- 5. Click on PROGRAM
- 6. Following programming, label the programmed EPLD.

1.4.1 Testing Suspect EPLDs

a. Initialize the PC with the Altera programmer per paragraph 1.3.a above.

b. If operating problems are appear to be related to U10, PLD200-x, Altera EPM7128LC84-3

- 1. EPLD listing found in H:\CONKLING\D09\PLD200\PLD200-x
- 2. Use personality module PLMJ7128-84-00. Initialize Altera program with PLD200-x project.
- 3. VERIFY the EPLD with the Altera programmer. Check the displayed checksum against the device label, and project PLD200-x. This is a good, but not a complete EPLD test.

1.5 Component installation

REQUIRED EQUIPMENT:

- 1 - 3X magnifying glass
- 1 - multimeter
- 1 - PLCC removal tool such as QILEXT-1

Using the assembly drawings D09-E2550-3, V196, or D09-E2550-2, V197, install U10. Check orientation as inserted.

WARNING: Use tool part number QILEXT-1 to remove the PLCC integrated circuit if necessary.

a. Perform a visual check of each integrated circuit for proper orientation, or bent pins.

b. Using the assembly drawings, D09-E2550-3, V196, D09-E2550-2, V197, or D09-E2550-1, V196 perform a final visual inspection of the assembled module permanent jumper patches.

V196 - JP1, JP3, JP6, JP9, JP11
V197 - JP9, JP11
V198 - JP5

c. Using the assembly drawings, D09-E2550-3, V196, D09-E2550-2, V197, or D09-E2550-1, V196 perform a final visual inspection of the assembled VME module.

d. With all the components installed, test for a short between the GROUND and +5V planes (C23-24 leads are a good place).

1.6 Initial power application

REQUIRED EQUIPMENT:

1 - BICC-Vero 6U extender board, modified to isolate +5V (preferred)
or
Kerner VME DEBUGGING ISOLATION BOARD, Assembly D09-E2386-5
1 - Current limiting 5 VDC, 5A power supply.
1 - multimeter
1 - RHIC timeline VME test chassis (modified with V101 bus)
or
AGS timeline VME chassis (modified with V101 bus)

WARNING: The VME chassis power supply can supply 120 A @ 5 VDC. Be careful with test lead ground clips etc.. Use the Kerner VME DEBUGGING ISOLATION BOARD, Assembly D09-E2386-5, to isolate Vcc and reduce risk of board damage.

a. Check that the RHIC timeline VME test chassis primary power switch is turned off.

b. Remove all VME modules from the RHIC timeline VME test chassis.

c. Obtain a modified BICC-Vero 6U extender board or VME debugging isolation assembly D09-E2386-5, and a 5V 5A power supply with current limiting.

1. Set the power supply to 5.0VDC.
2. Set the power supply current limit to 2 ADC.
3. Connect the power supply to the isolation board power supply cable.

d. On bench, install a module in the isolation assembly, and apply primary power to the isolation assembly D09-E2386-5 power supply.

1. Check the current drawn by the Modules. It should be no more than:
 - V196 300-400 mADC
 - V197 300-400 mADC
 - V198 200-300 mADC

WARNING: If the power supply current limits - immediately turn off the primary power, and check for shorts or reversed insertion of integrated circuits.

2. During the power test, no front panel LEDs should be illuminated. However, the front panel LEDs may flash as power is

turned on.

3. Check the integrated circuits for excessive heating (excessive means: cannot hold finger on circuit while operating), indicating (DIP) reverse insertion in the module.

g. If primary power checks, turn off the isolation assembly D09-E2386-5 power supply.

h. If installing modules in the RHIC timeline VME test chassis. The module positions are:

- V196 front slots 1-4
- V197 front slots 6-21
- V198 front slot 5 (only one module at a time)

Install transition modules in the RHIC timeline VME test chassis. The module positions are:

- T196 rear slots 1-4 (one required for each V196 module)
- T198 rear slot 5

If installing modules in the AGS timeline VME test chassis. The module positions are:

- V196 front slots 1-12
- V197 front slots 14-21
- V198 front slot 13 (only one module at a time)

Install transition modules in the RHIC timeline VME test chassis. The module positions are:

- T196 rear slots 1-12 (one required for each V196 module)
- T198 rear slot 13

i. Apply primary power to the VME test chassis.

1. The RHIC timeline VME test chassis power LEDs should be illuminated. The AGS timeline VME chassis does not contain power LED indicators.

2. The V196/V197 front panel LEDs should not be illuminated. However, the front panel LEDs may flash as power is turned on.

j. Burn-in power application

1. Note the approximate time. Leave modules in burn-in chassis for a minimum of 24 hours.

NOTE: Check for excessive heating after 15 minutes, and 1 hour of operation.

2. At end of burn-in period, check the VME test chassis primary power switch is turned off.

3. If additional modules must be burned in, remove burned in modules from the VME chassis.

4. Repeat procedure for all modules in test lot.

1.7 Initial V100 Timeline Encoder Module VMEbus tests

REQUIRED EQUIPMENT:

- 1 - Timeline VME test chassis (modified with V101 bus).
- 1 - Motorola model MVME162 host CPU in slot 1 set as TARGET3.
- 1 - LAN connection for host CPU.
- 1 - Console CRT w/null modem cable.
- 1 - V102 RHIC Timeline Delay Module.
- 1 - V196 AGS Timeline Decoder Module (For V196 test only).

- 1 - T196 AGS Timeline Decoder Transition Module (For V196 test only).
- 1 or more - V197 AGS Timeline Trigger Modules.
- 1 - V198 AGS Timeline Buffer Module.
- 1 - T196 AGS Timeline Trigger Transition Module.
- 1 - V199 Passive Load Module.
- 1 - Digital Oscilloscope w/probes.
- 1 - D09-E2530 Fanout Assembly Test Box.
- 1 - Coaxial cable with BNC connectors, and adaptor BNC to K-lock.
- 1 - Twin-axial cable with twin-BNC connectors, approximately 36-48 inches.
- 8 - Timing coaxial cables with K-lock connectors, approximately 24-36 inches.
- 1 - Laboratory AGS real time generator.
- 1- Ribbon cable, 25-wire, with two DB25P connectors, long enough to reach the laboratory AGS real time generator.

1.7.1 V196 AGS Timeline Decoder Module tests

NOTE: The V196 AGS Timeline Decoder Module is installed in a VME chassis. However, its only connection to the VMEbus is +5V and GND. No VMEbus connections are made except for P1 interrupt and bus grant pass through.

- a. Check the VME test chassis primary power switch is turned off.
- b. Install the MV162 module in slot 1, and set the MV162 host computer for VxWorks. Install LAN adapter and connect laboratory LAN cable.
- c. Install the V102 module in slot 2. No Timeline cable required.
- d. Install the V199 module in slot 21.
- e. Install V196 modules under test in slots 3-4. Install T196 modules in the rear slots 3-4.
- f. Apply primary power to the RHIC timeline VME test chassis.
 - 1. The RHIC timeline VME test chassis power LEDs should be illuminated.
 - 2. The MV162 front panel LEDs should be illuminated. The V102 OFFLINE Led should illuminate, and the V196 LEDs should not illuminate. However, the front panel LEDs will flash as power is turned on.
- g. When VxWorks and the startup script are completed set the V102 module:
 - 1. ONLINE (0xffffe641 = 0x01).
 - 2. Channels 1, 3, 5, & 7 to external trigger:
 - 0xffffe648 = 0x00, 0x00, 0x00, 0x01, 0x00, 0x01, 0x22, 0x00
 - 0xffffe658 = 0x00, 0x00, 0x00, 0x01, 0x00, 0x01, 0x22, 0x00
 - 0xffffe668 = 0x00, 0x00, 0x00, 0x01, 0x00, 0x01, 0x22, 0x00
 - 0xffffe678 = 0x00, 0x00, 0x00, 0x01, 0x00, 0x01, 0x22, 0x00

The V102 module will properly load the V196 outputs, and indicate a trigger.

h. Connect the D09-E2530 Fanout Assembly Test Box power cable to the V199 front panel +5V and GND test points for power. Connect its output to the V196 under test T196 transition module twin-BNC input connector. Set the Fanout Test Box to COUNT.

- 1. All 16 LEDs on the V196 under test should illuminate.
- 2. In groups of 4 connect the V196 outputs to the V102 external

inputs:

- The V102 LEDs for channel 1, 3, 5, & 7 should illuminate at the same time as the V196 output is triggered.
- Repeat groups of 4 until the 16 V196 outputs are tested.

i. Set the D09-E2530 Fanout Test Box to SWITCH. Obtain the listing for U10, PLD200-x. Using the listing:

1. Set all 16 event codes in the Fanout Test Box switch register.
 - Check that the LED for the event code in the switch register illuminates.

1.7.2 V197/V198 AGS Timeline Trigger/Buffer Module tests

NOTE: The V197/V198 AGS Timeline Trigger/Buffer Modules are installed in a VME chassis. However, the only connections are:

- P1 interrupt and bus grant pass through
- P1 & P2 VMEbus +5V and GND
- P2 user pins.

a. Check the VME test chassis primary power switch is turned off.

b. Install the MV162 module in slot 1, and set the MV162 host computer for VxWorks. Install LAN adapter and connect laboratory LAN cable.

c. Install the V102 module in slot 2. No Timeline cable required.

d. Install the V199 module in slot 21.

e. Install V198 modules under test in slot 5. Install T198 module in the rear slots 5.

f. Install V197 modules under test in slots 6-20.

g. Connect the output of the laboratory AGS real time generator to the T198 25-pin input connector. Using the Apollo spreadsheet, and the listing of U10, PLD200-x for the modules under test, program all event codes possible into the spreadsheet.

h. Apply primary power to the RHIC timeline VME test chassis.

1. The RHIC timeline VME test chassis power LEDs should be illuminated.
2. The MV162 front panel LEDs should be illuminated. The V102 OFFLINE Led should illuminate, and the V196 LEDs should not illuminate. However, the front panel LEDs will flash as power is turned on.

i. When VxWorks and the startup script are completed set the V102 module:

1. ONLINE (0xffffe641 = 0x01).
2. Channels 1, 3, 5, & 7 to external trigger:
 - 0xffffe648 = 0x00, 0x00, 0x00, 0x01, 0x00, 0x01, 0x22, 0x00
 - 0xffffe658 = 0x00, 0x00, 0x00, 0x01, 0x00, 0x01, 0x22, 0x00
 - 0xffffe668 = 0x00, 0x00, 0x00, 0x01, 0x00, 0x01, 0x22, 0x00
 - 0xffffe678 = 0x00, 0x00, 0x00, 0x01, 0x00, 0x01, 0x22, 0x00

The V102 module will properly load the V196 outputs, and indicate a trigger.

j. Start the laboratory AGS real time generator.

1. All 16 LEDs of each V197 under test should illuminate.
2. In groups of 4 connect the V197 outputs to the V102 external inputs:
 - The V102 LEDs for channel 1, 3, 5, & 7 should illuminate at the same time as the V196 output is triggered.
 - Repeat groups of 4 until the V197 outputs are tested.

k. Set the laboratory AGS real time generator to generate one event code. Using the listings for U10, PLD200-x:

1. Set all event codes in the AGS real time spreadsheet - one at a time.
 - Check that the LED for the event code on the spreadsheet illuminates.